2.1 A 128×128 Single-Photon Imager with on-Chip Column-Level 10b Time-to-Digital Converter Array Capable of 97ps Resolution

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Time-resolved optical imaging has many uses in physics, molecular biology, medical sciences and computer vision, just to name a few. Deep sub-nanosecond timing resolution, in combination with high sensitivity, is becoming increasingly important in a number of imaging methods. Non solid-state devices enabling picosecond time resolution, such as photomultiplier tubes and microchannel plates, have existed for decades. However, cost and size have limited their use to low-scale and scientific applications. In solid-state technology, single-photon avalanche diodes (SPADs) have become the alternative of choice [1]. Recently, SPADs are even more compelling with the emergence of CMOS implementations [2] and the appearance of multi-pixel designs [3]-[6].

With the growth of the array size however, it has become increasingly hard to process massive volumes of data from SPAD pixels. To address this issue, hybrid systems have been proposed that combine advanced CMOS technologies with processes designed to optimize SPAD performance [7]. The main limitation of this approach is the increased complexity of fabrication and, possibly, higher costs. Analog design techniques have also been used to evaluate the photon's time-of-arrival (TOA) on-chip [5]. However, increased pixel size and potentially complex schemes to compensate for temperature and technological variability are often needed.

We present an array of 128×128 highly miniaturized SPAD pixels with a bank of 32 time-to-digital converters (TDCs) on chip. The block diagram of the system is shown in Fig. 2.1.1. A decoder selects a 128-pixel row. Every group of 4 pixels in the row shares a TDC based on an event-driven mechanism similar to [4]. As a result, row-wise parallel acquisition is obtained with a low number of TDCs. Thanks to the outstanding timing precision of SPADs and an optimized TDC design, a typical resolution of 97ps is achieved within a range of 100ns (10b) at a maximum rate of 10MS/s per TDC. The TDC bank exhibits a DNL of 0.08LSB and an INL of 1.89LSB.

Figure 2.1.2 (a) shows the pixel schematics based on a configuration with seven NMOS transistors. The SPAD, implemented as a p+/p-well/deep n-well junction, is based on [4], where detailed device characterization is reported. The breakdown voltage V_{BD} of the SPAD in this design is 17.7V. At its cathode, a bias voltage of 21V is applied in order to operate with an excess bias voltage V_E of 3.3V. A row selection transistor (M_1) decouples the SPAD anode from pixels in the columns that are not selected. At the selected row, the SPAD is charged as a result of its anode being connected to ground via quenching/recharge transistor M_2. Transistors M_3, M_4, and M_6 operate as switches to set V_{GS} of M_2 to either V_{QCH} or V_{RCH} in order to quench the avalanche or recharge the SPAD. M_5 is used as a capacitor to reduce the effect of switching noise on V_{QCH} caused by charge injection from the gate of M_2. M_7 is the pixel output transistor. It operates as a pull-down for the column line when a photon is detected. The column line potential is kept high by pull-up transistors at the bottom of the column.

Figure 2.1.2 (b) shows a simplified block diagram of the TDC. Time-to-digital conversion is obtained as a result of an interpolation of three delay measurements: coarse, medium, and fine. The main TDC structure is similar to [8]. Nonetheless, further improvements have been implemented to reduce the silicon area and perform flash conversion, thus increasing throughput. Each TDC has an independent controller that is used as a time interpolator, to generate internal signals and to control its operating mode. Each controller also manages the interface with the global readout circuit and the column circuitry. A global master DLL generates 16 uniformly spaced phases PHI[15:0] based on a global CLK/START signal. Example waveforms for CLK/START and PHI are shown in Fig. 2.1.2(c). The input frequency of the master DLL is typically 40MHz, thus τ_C is 25ns for time interval measurements. The time separation between two successive phases sets τ_M to 1.5625ns.

The TDC supports two main operating modes: (i) a measurement mode and (ii) a calibration mode. In measurement mode, the STOP signal originated by the first of four SPADs that detects a photon is mapped to signal TRG in column-level TDC. A 2b counter clocked by signal CLK delivers coarse resolution τ_C for a measurement range of $4\tau_C$. Medium resolution τ_M is achieved by finding that pair of global phases PHI which delimits the transition of TRG. The register used for τ_M also generates a synchronization signal SYNC that is precisely asserted on the second phase transition following the rising edge of TRG. The time delay between TRG and SYNC is measured by means of a 32-tap delay line and register, which are designed based on the TDC core of [9]. In the TDC interpolator, the three measurements, delivering 2, 4, and 4 bits of resolution, are combined into the total time delay code. Only 16 delay cells (4b) of the fine delay line are used for the final result. The remaining delay cells are added to accommodate timing shifts due to process, voltage or temperature variations.

In calibration mode, the TDC utilizes the full 32-tap fine delay line as a local DLL that locks to two non-successive phases (PHI[i] and PHI[i+2]) with a total duration of $2\tau_M$, thus generating a fine resolution τ_F of 97.66ps. The analog control voltage of the DLL is stored on a local capacitor. Since calibration is performed individually in each TDC, matching requirements between TDCs may be relaxed. The output of all TDCs is transferred off-chip via a fast global readout circuit consisting of 32 TDC interface blocks, a configuration/testing JTAG controller and a pipelined time-multiplexer readout chain. The readout circuit controls 8 digital 12b output buses. Each bus provides the 10b TDC data and 2b column address to identify the originator of the STOP signal among four pixels. In order to maximize data rate, the readout circuit operates four times faster than the TDC frequency. To reduce power consumption, IO pads only change state when valid data are available in a readout cycle. The readout circuit also provides configuration/testing measures to read and modify most TDCs and readout circuit registers via an integrated JTAG controller.

The chip micrograph is shown in Fig. 2.1.3 along with a detail of the pixel. The pixel measures 25×25μm^2. The sensor was tested in three steps. First, the TDCs were characterized separately. Second, the TDC array was operated in measurement mode and connected with the SPAD array when exposed to ambient light. The performance of the TDC bank is summarized in Fig. 2.1.4. The figure shows the worst-case DNL and INL measured over the entire bank over several days, to verify the effectiveness of calibration over temperature and technological variations. Finally, the chip was exposed to direct pulsed laser illumination generated by a 637nm solid-state laser source. The pulses were 80ps wide with a repetition rate of 40MHz. The power of the laser was adjusted to minimize pile-up distortion and a TOA histogram was built for each pixel. The resulting jitter measurements, along with the dark count rate (DCR), are shown in Fig. 2.1.5.

The chip's overall performance was tested in a breadboard system based on an FPGA. The breadboard was designed to provide all the digital interface signals and memory support for the imager output. The sensor imaged a 3D scene illuminated by a pulsed laser. Figure 2.1.6 shows the 3D image obtained using the same techniques as in [3], whereby the total integration time for one frame was 1s, with a worst-case distance error of 1.4mm. Fig. 2.1.7 is a performance summary of the sensor chip and its various components. This research was supported by a grant from the Swiss National Science Foundation. The authors are grateful to Maximilian Sergio for help during the IC tape-out.

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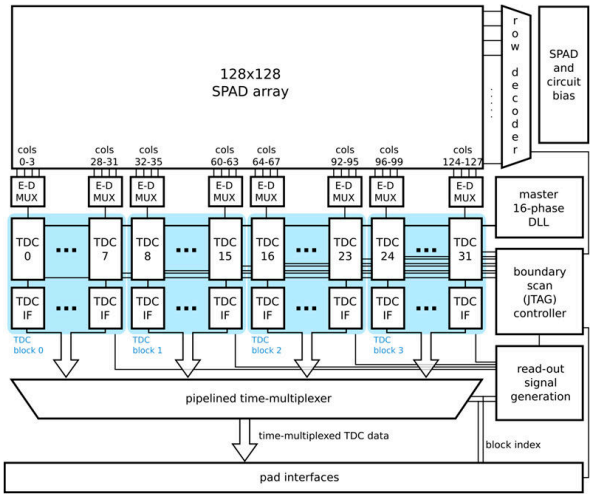

Figure 2.1.1: Block diagram of the proposed sensor. The sensor consists of a 128x128 pixel array, a bank of 32 TDCs, and a fast parallel readout circuitry. A row decoding logic selects 128 pixels that are activated for detection. The pixels are organized in groups of four that access the same TDC based on a first-in-take-all sharing scheme.

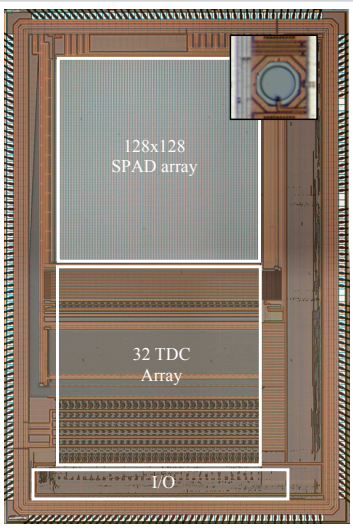

Figure 2.1.3: Photomicrograph of the sensor chip with a pixel detail in the inset. The circuit, fabricated in 0.35μm CMOS technology, has a surface of 8x5mm². The pixel pitch is 25μm.

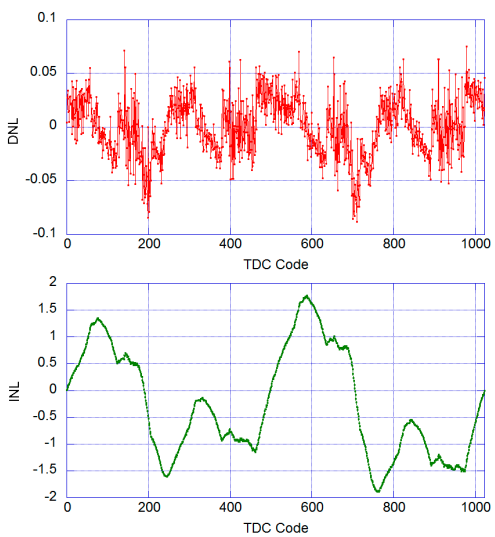

Figure 2.1.4: Measurements of differential non-linearity (DNL) and integral non-linearity (INL) for the worst case TDC at room temperature.

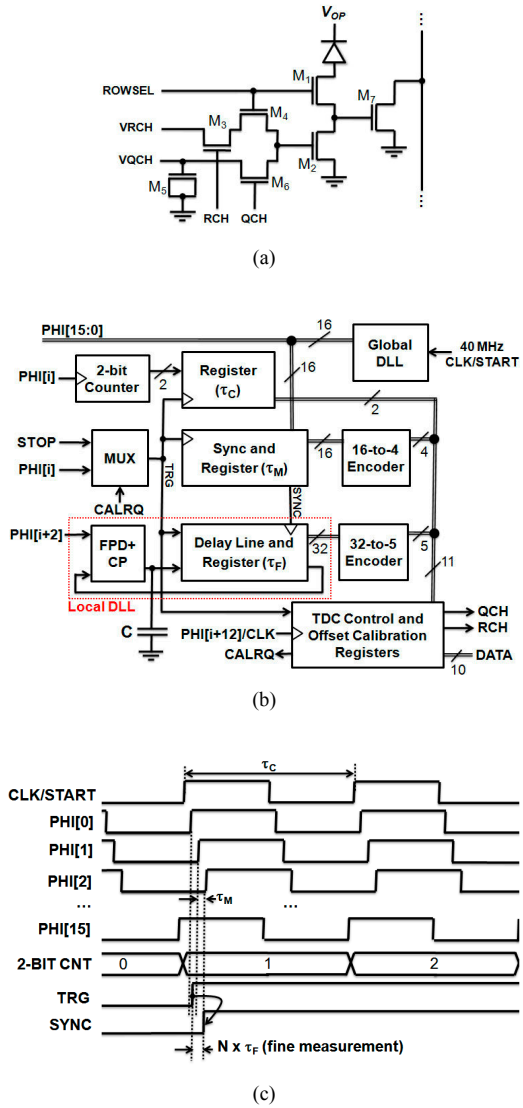

Figure 2.1.2: (a) Pixel schematic. (b) Simplified TDC block-diagram. (c) TDC signal waveform.

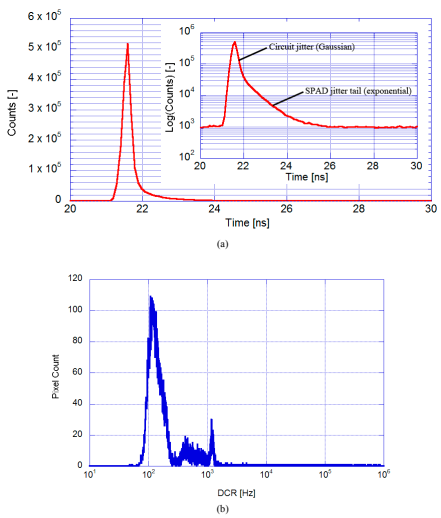

Figure 2.1.5: (a) Time jitter measurement of the SPAD detector and overall circuitry using the integrated TDCs. In the inset, a logarithmic plot is shown. The illumination laser pulse width was 80ps. (b) Dark count rate (DCR) distribution over the array.

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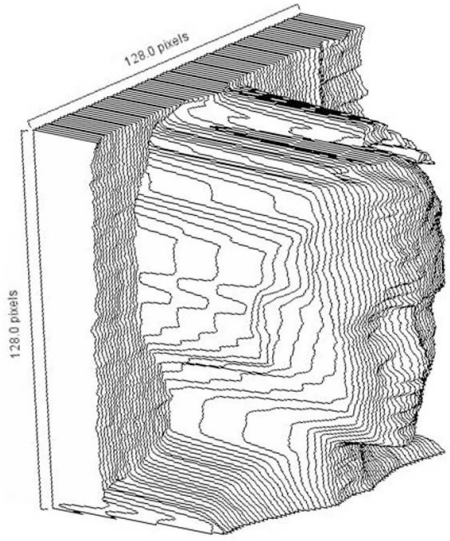

Figure 2.1.6: Experimental 3D image with model picture in inset. The 1σ error computed from two subsequent images is 1.4mm.

	Parameter	Symbol	Min.	Typ.	Max.	Unit
Pixel	Photon detection probability @ V_e=3.3V	η	3		35 @ 460nm	%
	Photon detection probability @ V_e=4.0V	η	3		40 @ 460nm	%
	Sensitivity spectrum	λ	350		800	nm
	Median DCR			284		Hz
	Dead time	τ_{DT}		100		ns
TDC	Tuning of measurement range (10 bits)		71.68	100	204.8	ns
	Resolution (LSB)	τ_r	70	97.66	200	ps
	Measurement rate				10	MS/s
	DNL			0.08		LSB
	INL			1.89		LSB
System	Clock frequency		19.5	40	55.8	MHz
	Total IO bandwidth			7.68		Gbps
	JTAG bandwidth			8		Mbps
	Static power dissipation			33		mW
	Dynamic power dissipation			150		mW
3D Image Sample	Integration time			1		s
	Illumination average power			1		mW
	Illumination peak power			250		mW
	Illumination duty cycle			0.4		%
	Target area			1		m^2
	Target distance @40MHz		0.1	1.5	3.75	m

Figure 2.1.7: Performance summary for the image sensor.

